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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,658	07/29/2003	Dan Case	15436.118.1.1	6499

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EXAMINER

SEDIGHIAN, REZA

ART UNIT	PAPER NUMBER
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2613

DATE MAILED: 09/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

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<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/629,658	CASE ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	M. R. Sedighian	2613	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 29 July 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-46 is/are pending in the application.  
     4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 38-40 is/are allowed.
- 6) ☒ Claim(s) 1-17, 19-27, 29-37 and 41-46 is/are rejected.
- 7) ☒ Claim(s) 18 and 28 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
     a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>8/9/04, 2/2/04</u> .  | 6) <input type="checkbox"/> Other: _____                                    |

### Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1, 2, 3, 7, 8, 11, 18, 20, 24, 28, 29, 31, 32, 33, 34, and 35 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 10, 12, 13, 14, 16, 19, 20, 21, 22, 23, 24, 33, 34, 35, 36, and 37 of copending Application No. 10/282,579. Although the conflicting claims are not identical, they are not patentably distinct from each other because both application claim an integrated post-amplifier and laser driver assembly for use in conjunction with an optical receiver and an optical transmitter, comprising of a post-amplifier assembly that is configured for communication with the optical receiver, a laser driver assembly implemented together with the post-amplifier in a single IC and being configured to communicate with the optical transmitter, and a digital control interface in communication with the post-amplifier assembly and the laser driver assembly.

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This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-17, 19-27, 29-35, and 36-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Aronson et al. (US Patent No: 2002/0149821 A1).

Regarding claims 1, 11, and 20, Aronson teaches an integrated post-amplifier and laser driver assembly (100, fig. 2) for use in conjunction with an optical receiver (102, fig. 2) and an optical transmitter (103, fig. 2), comprising: a post-amplifier assembly (104, fig. 2) configured for communication with the optical receiver (102, fig. 2); a laser driver assembly (105, fig. 2) configured for communication with the optical transmitter (103, fig. 2); a digital control interface (controller IC, figs. 2, 3) in at least indirect communication with the post-amplifier assembly and the laser driver assembly (page 3, paragraph 0032); and means for setting a signal parameter (134, fig. 3) in response to signal parameter programming instructions (page 3, paragraphs 0029, 0032), the signal parameter corresponding to a signal associated with at least one of the post-amplifier assembly, and the laser driver assembly (page 3, paragraph 0032). As to claim 11, Aronson teaches a glue logic module (logic 134, fig. 3) in communication with the digital control interface (120, fig. 3) and a digital to analog converter (123-1, fig. 3) and configured to receive

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signal parameter programming instructions concerning the setting of a signal parameter and being in communication with glue logic module and at least one of the post-amplifier and laser driver assembly (page 3, paragraphs 0029, 0032). As to claim 20, Aronson further teaches an optical transmitter (103, fig. 2) and an optical receiver (102, fig. 2).

Regarding claims 2 and 29, Aronson teaches the post-amplifier assembly (104, fig. 2) and laser driver assembly (105, fig. 2) are integrated together in a single IC (100, fig. 2).

Regarding claim 3, Aronson teaches the means for setting a signal parameter (134, fig. 3) enables dynamic control of one or more signal parameters (page 2, paragraph 0017 and page 3, paragraph 0029).

Regarding claims 4 and 21, Aronson teaches the means for setting a signal parameter operates in response to signal parameter programming instructions received, at least indirectly, from one of a user and an algorithm encoded within the integrated post-amplifier and laser driver assembly (page 4, paragraph 0035 and 124, 134, fig. 3).

Regarding claim 5, Aronson teaches the means for setting a signal parameter enables implementation of a signal parameter change that corresponds to a change in thermal conditions associated with the integrated post-amplifier and laser driver assembly (page 1, paragraph 0011, page 2, paragraph 0020, page 3, paragraph 0033).

Regarding claims 6, 15, and 22, Aronson teaches the signal to which the signal parameter corresponds is selected from the group consisting of: control signals, data signals, power signals, and monitor signals (page 1, paragraph 0007, page 3, paragraphs 0030, 0032).

Regarding claim 7, Aronson teaches the digital control interface comprises a serial digital interface (page 3, paragraph 0028 and 121, fig. 3).

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Regarding claim 8, Aronson further teaches means for controlling signal polarity (133, fig. 3) arranged for operation with respect to a data signal associated with the integrated post-amplifier and laser driver assembly (page 4, paragraphs 0036, 0043).

Regarding claims 9, 17, and 27, Aronson further teaches a feedback loop configured and arranged for operation with respect to the signal to which the signal parameter corresponds (page 4, paragraph 0035, note that controller 110 uses monitoring information to provide diagnostic feedback to the host device by incorporating logic 134 and multiplexer 124).

Regarding claims 10, 19, and 36-37, Aronson further teaches the integrated post-amplifier and laser driver assembly is compatible with a plurality of protocols and line rates (page 1, paragraph 10, page 4, paragraph 0045).

Regarding claim 12, Aronson further teaches the digital to analog converter is configured to receive signal parameter programming instructions from at least one of a user, or an algorithm encoded within the integrated post-amplifier and laser driver assembly (page 3, paragraph 0032).

Regarding claim 13, Aronson further teaches the signal parameter programming instructions concern LOS assert and deassert thresholds (page 3, paragraph 0027, page 4, paragraphs 0040, 0041).

Regarding claims 14 and 23, Aronson further teaches the signal parameter is selected from the group consisting of: signal rise time, signal polarity, signal assert threshold, signal deassert threshold, signal fall time, signal amplitude, and signal power (page 1, paragraph 0007, page 3, paragraphs 0030, 0032, page 4, paragraphs 0040, 0043).

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Regarding claims 16 and 26, Aronson further teaches an LOS circuit (133, fig. 3) in at least indirect communication with the optical receiver and the digital control interface (page 4, paragraphs 0040, 0041).

Regarding claim 24, Aronson teaches a glue logic module (logic 134, fig. 3) in communication with the digital control interface (120, fig. 3) and a digital to analog converter (123-1, fig. 3) and configured to receive signal parameter programming instructions concerning and being in communication with glue logic module and at least one of the post-amplifier assembly and laser driver assembly (page 3, paragraphs 0029, 0032).

Regarding claim 25, Aronson further teaches the digital to analog converter is configured to receive signal parameter programming instructions from at least one of a user, or an algorithm encoded within the integrated post-amplifier and laser driver assembly (page 3, paragraph 0032).

Regarding claim 30, Aronson further teaches the digital IC controller includes a 12C bus through which signal parameter programming instructions can be passed (for example, the signal lines that connects controller IC 110 to the laser driver 105).

Regarding claims 31-32, Aronson further teaches the optical receiver comprises a receive optical subassembly (ROSA 2, fig. 1 and ROSA 102, fig. 2) that comprises of a transimpedance amplifier and a photodiode in communication with the amplifier (page 1, paragraph 0013).

Regarding claims 33-35, Aronson further teaches the optical transmitter comprises a transmit optical subassembly (TOSA 3, fig. 1 and ROSA 103, fig. 2) that comprises of a laser and a laser driver in communication with the laser (page 1, paragraph 0013).

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5. Claims 41-46 are rejected under 35 U.S.C. 102(e) as being anticipated by Chieng et al. (US Patent No: 6,862,302 B2)

Regarding claim 41, Chieng teaches a computer program product for implementing a method for controlling the performance of an optical transceiver (100, figs. 2, 5 and col. 1, lines 10-13, 65-67, col. 2, lines 1-8), comprising: a computer readable medium (804, fig. 5) carrying computer executable instructions for performing the method (col. 8, table 1, step 1), wherein the method comprises: accessing information concerning a signal parameter corresponding to a signal associated with the optical transceiver (table 1, step 1); setting the signal parameter to a value consistent with the information thus accessed (table 1, step 1); and repeating if required the process of accessing information and the process of setting the signal parameter (table 1, step 2a, step 17).

Regarding claim 42, Chieng teaches the accessing information and the setting signal parameter processes are performed automatically as a result of the occurrence of a predefined event (col. 8, table 1, steps 2a, 2b).

Regarding claim 43, Chieng teaches the predefined event comprises one of a line rate change, and a change in thermal conditions associated with the optical transceiver (col. 1, lines 9-12, col. 5, lines 24-35 and col. 9, table 1, steps 8, 9, 11).

Regarding claim 44, Chieng teaches the signal parameter is selected from the group consisting of signal rise time, signal polarity, signal assert threshold, signal deassert threshold, signal fall time, signal amplitude, and signal power (col. 6, lines 16-23, col. 24, lines 18-20 and table 1, steps 2a, 2b, 6).



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Regarding claim 45, Chieng teaches the signal to which the signal parameter corresponds is selected from the group consisting of control signals, data signals, power signals, and monitor signals (col. 2, lines 10-47 and table 1, steps 2a, 2b).

Regarding claim 46, Chieng further teaches accessing feedback information concerning the signal parameter (col. 2, lines 10-17, col. 5, lines 45-51); and using the feedback information to facilitate maintenance of the signal parameter within a predetermined range of the set value until a resetting of the signal parameter occurs (table 1, steps 2a, 2b, 5).

6. Claims 38-40 are allowed over prior art of record.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. R. Sedighian whose telephone number is (571) 272-3034.

The examiner can normally be reached on M-F (from 9 AM to 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on (571) 272-3022. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would

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like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

  
M. R. SEDIGHIAN  
PRIMARY EXAMINER